Examination is respectfully requested.

Respectfully submitted,

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MARKED UP VERSION OF REPLACED PARAGRAPHS OF THE SPECIFICATION

Page 13, second full paragraph (lines 4-8), the marked-up paragraph is as follows:

Fig. 25 [is a photograph taken by a scanning electron microscope showing] illustrates a the prototype element having memory cells of 120 bits by repeatedly using the structure of the semiconductor element of Embodiment 6 of the present invention.

Pages 35 and 36, the paragraph bridging these pages from page 35, line 24 to page 36, line 12, the marked-up paragraph is as follows:

In Fig. 24, there is shown a structure in which four present structures are repeatedly arranged to have sixteen thin film regions. In Fig. 25, moreover, there is presented an [electron-microscope photograph] illustration of a prototype element which is prepared by arranging the present structures repeatedly and by arranging memory cells of 120 bits in a matrix. In the photograph, ten control electrodes run transversely. Six sets of three low-resistance regions run longitudinally (which correspond to the low-resistance regions 1 to 3 such that two of them correspond to the thin film regions 1 and 2 for one control electrode). There are

arranged 10 x 6 x 2 = 120 thin film regions. In this large-scale memory, the writing, erasing and reading methods can be accomplished basically in an identical manner.